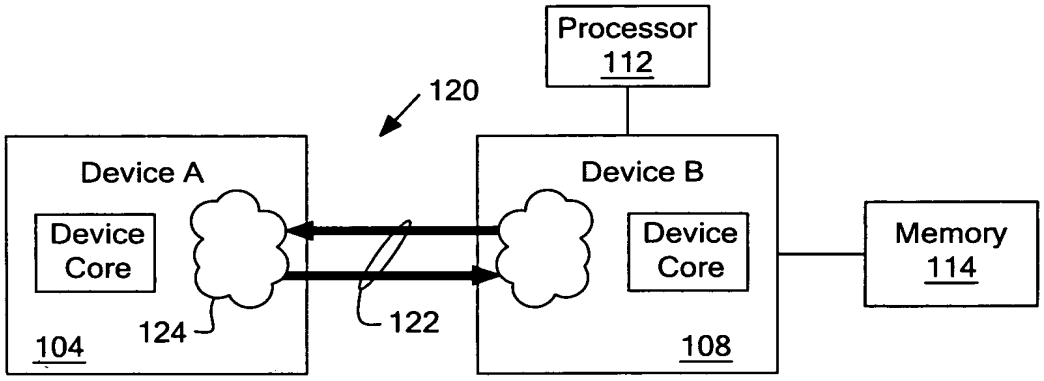
Processor
112
120
Device A
Device
Core
124
104
122
Device B
Device
Core
108
Memory
114

Fig.1

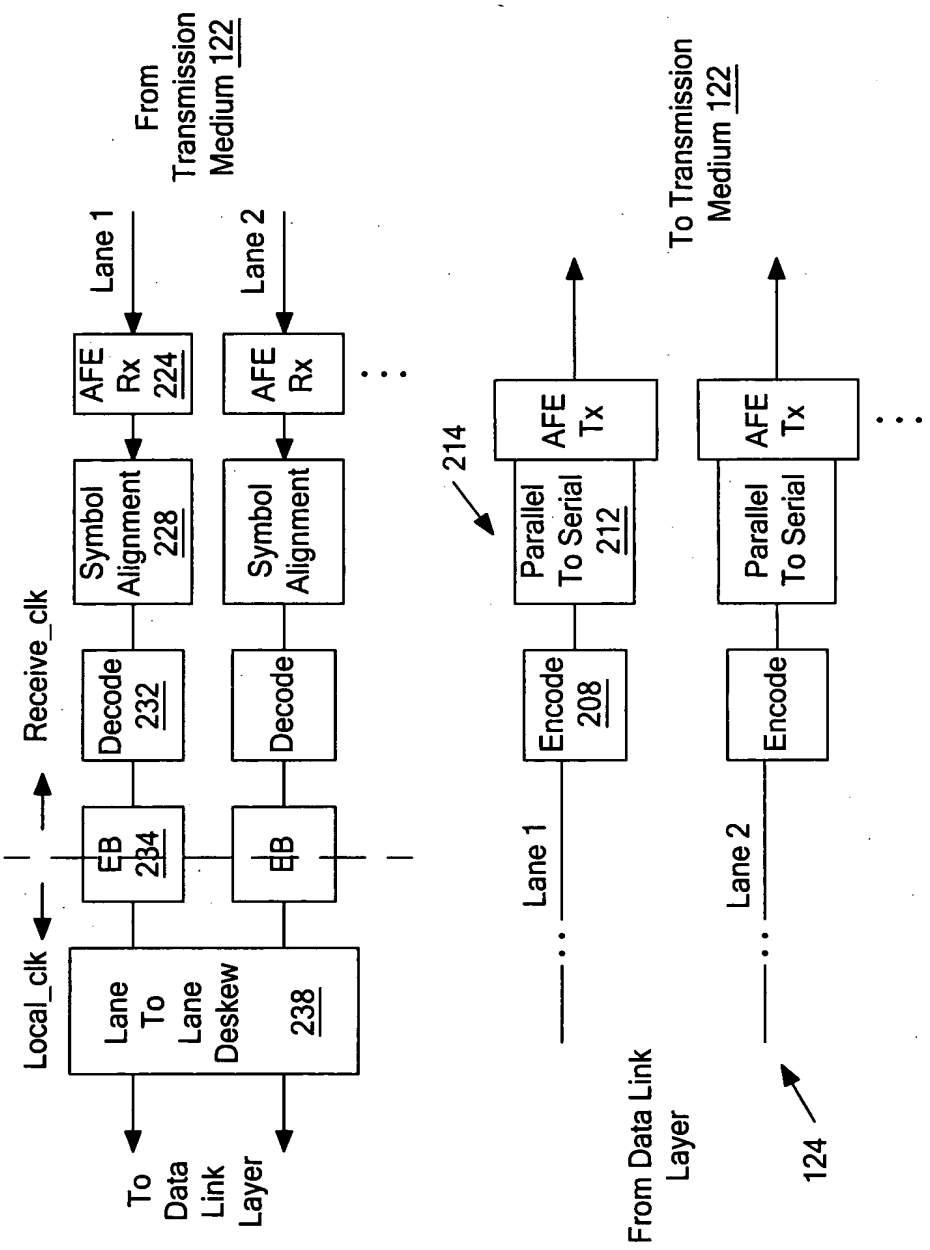
From Transmission Medium 122
Lane 1
Lane 2
AFE Rx 224
Symbol Alignment 228
Decode 232
EB 234
Receive_clk
Local_clk
Lane To Lane Deskew 238
To Data Link Layer
214
AFE Tx
Parallel To Serial 212
Encode 208
Lane 1
Lane 2
From Data Link Layer
124
To Transmission Medium 122

Fig.2

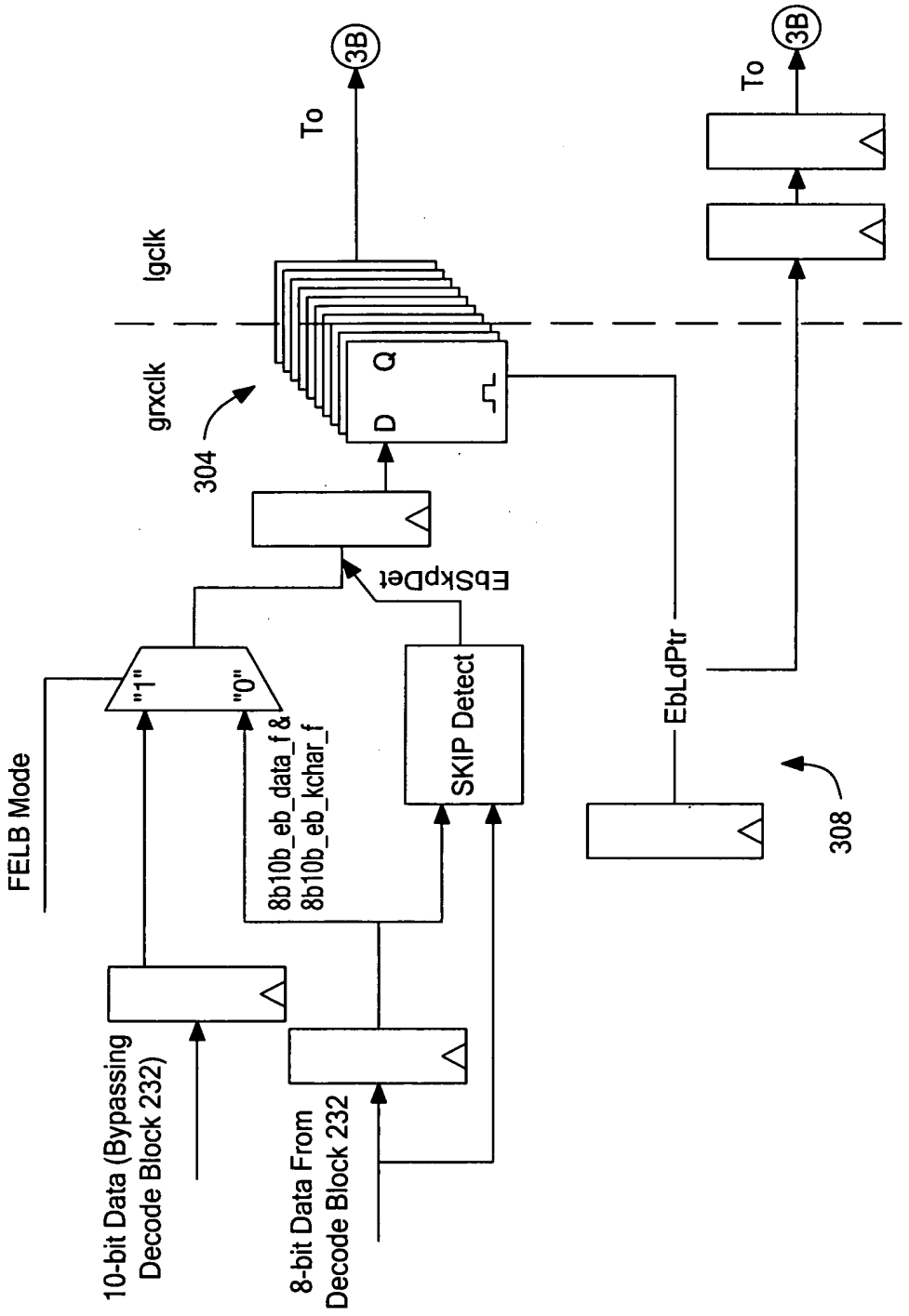
To
3B
To
3B
lgclk
grxclk
304
D
Q
EbSkpDet
"1"
"0"
FELB Mode
8b10b_eb_data_f &
8b10b_eb_kchar_f
SKIP Detect
EbLdPtr
308
10-bit Data (Bypassing Decode Block 232)
8-bit Data From Decode Block 232

Fig.3A

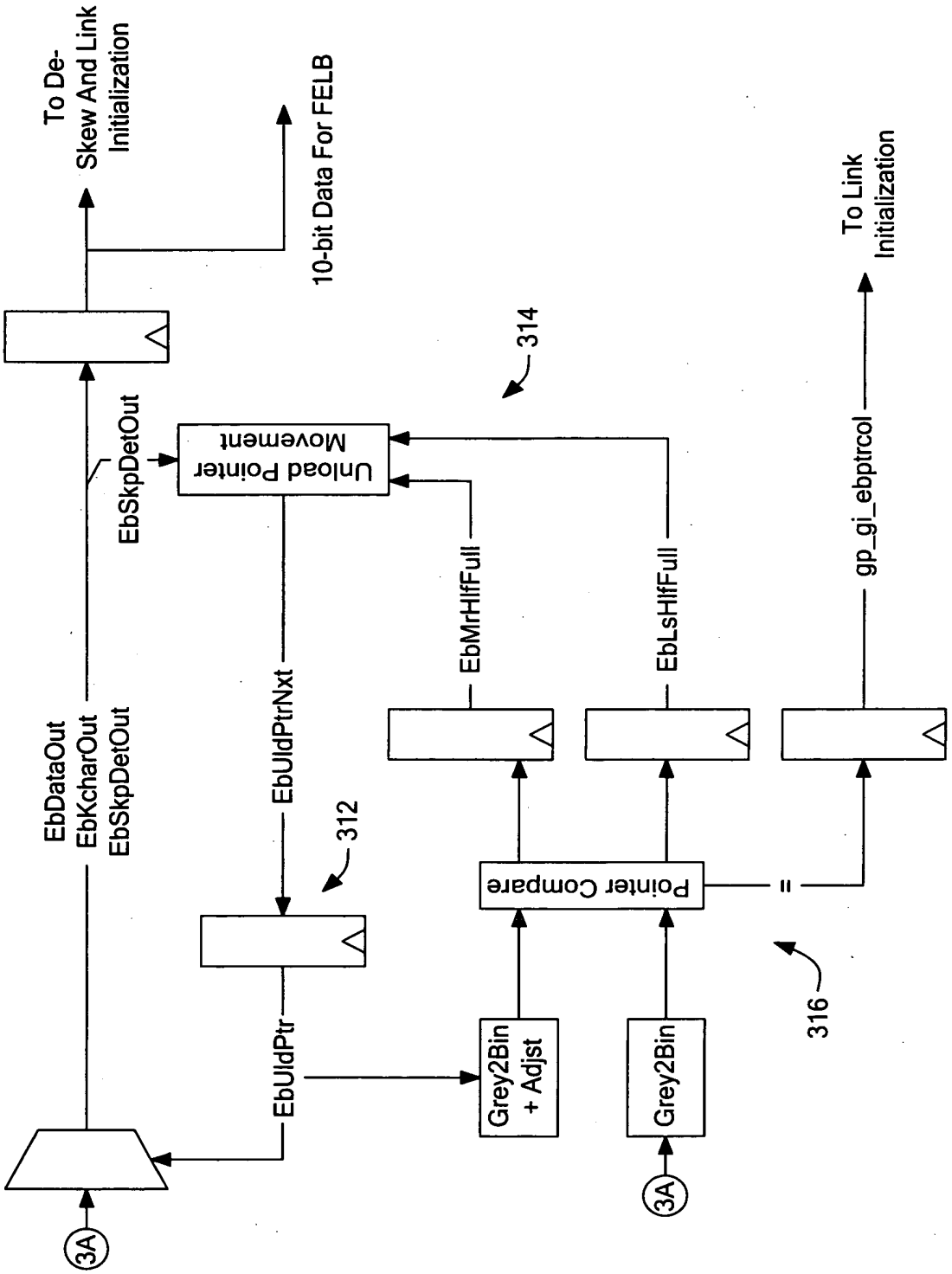
To De-Skew And Link Initialization
10-bit Data For FELB
314
EbSkpDetOut
Unload Pointer Movement
EbMrHlfFull
EbLsHlfFull
gp_gi_ebptrcol
To Link Initialization
EbDataOut
EbKcharOut
EbSkpDetOut
EbUldPtrNxt
312
Pointer Compare
=
316
EbUldPtr
Grey2Bin + Adjst
Grey2Bin
3A
3A

Fig.3B

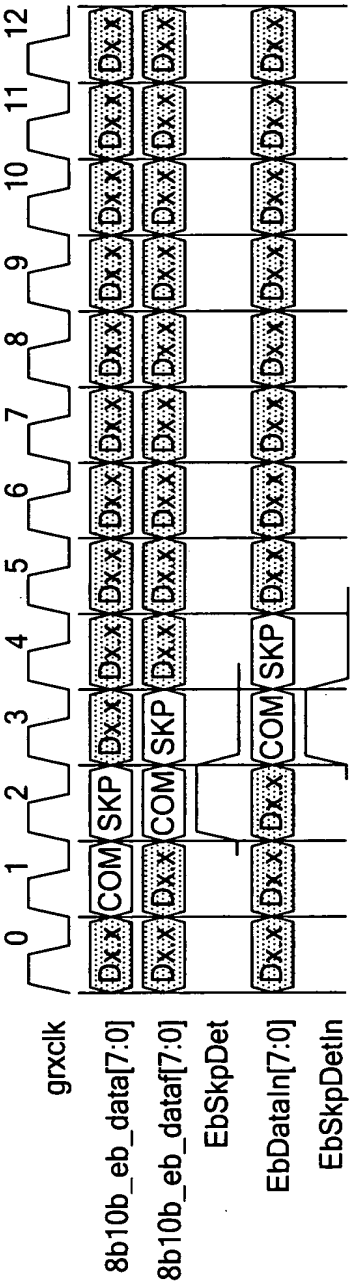
0
1
2
3
4
5
6
7
8
9
10
11
12
grxclk
8b10b_eb_data[7:0]
8b10b_eb_dataf[7:0]
EbSkpDet
EbDataIn[7:0]
EbSkpDetIn
COM
SKP
Dx.x

Fig.4

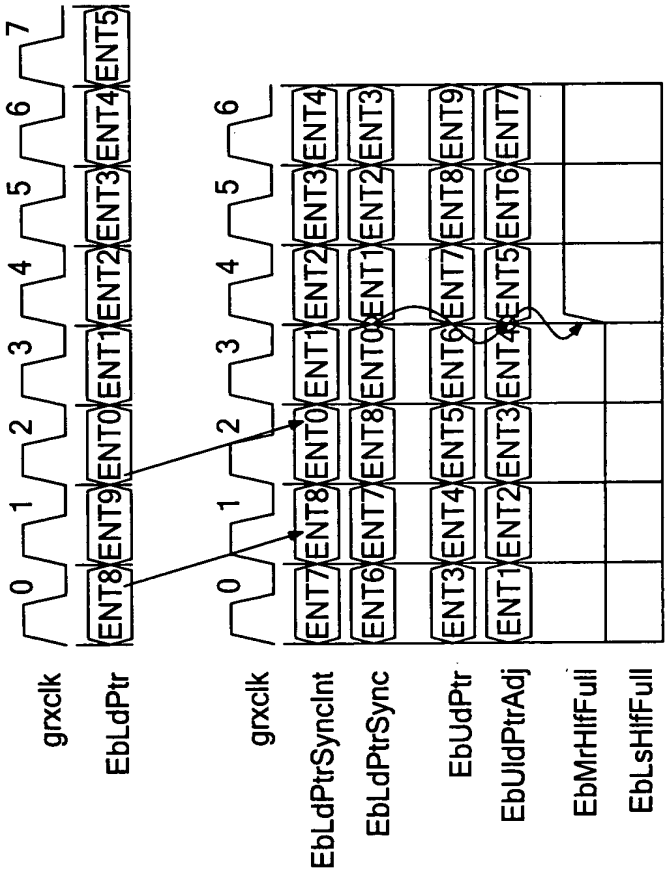
grxclk
EbLdPtr
grxclk
EbLdPtrSyncInt
EbLdPtrSync
EbUdPtr
EbUldPtrAdj
EbMrHlfFull
EbLsHlfFull

Fig.5

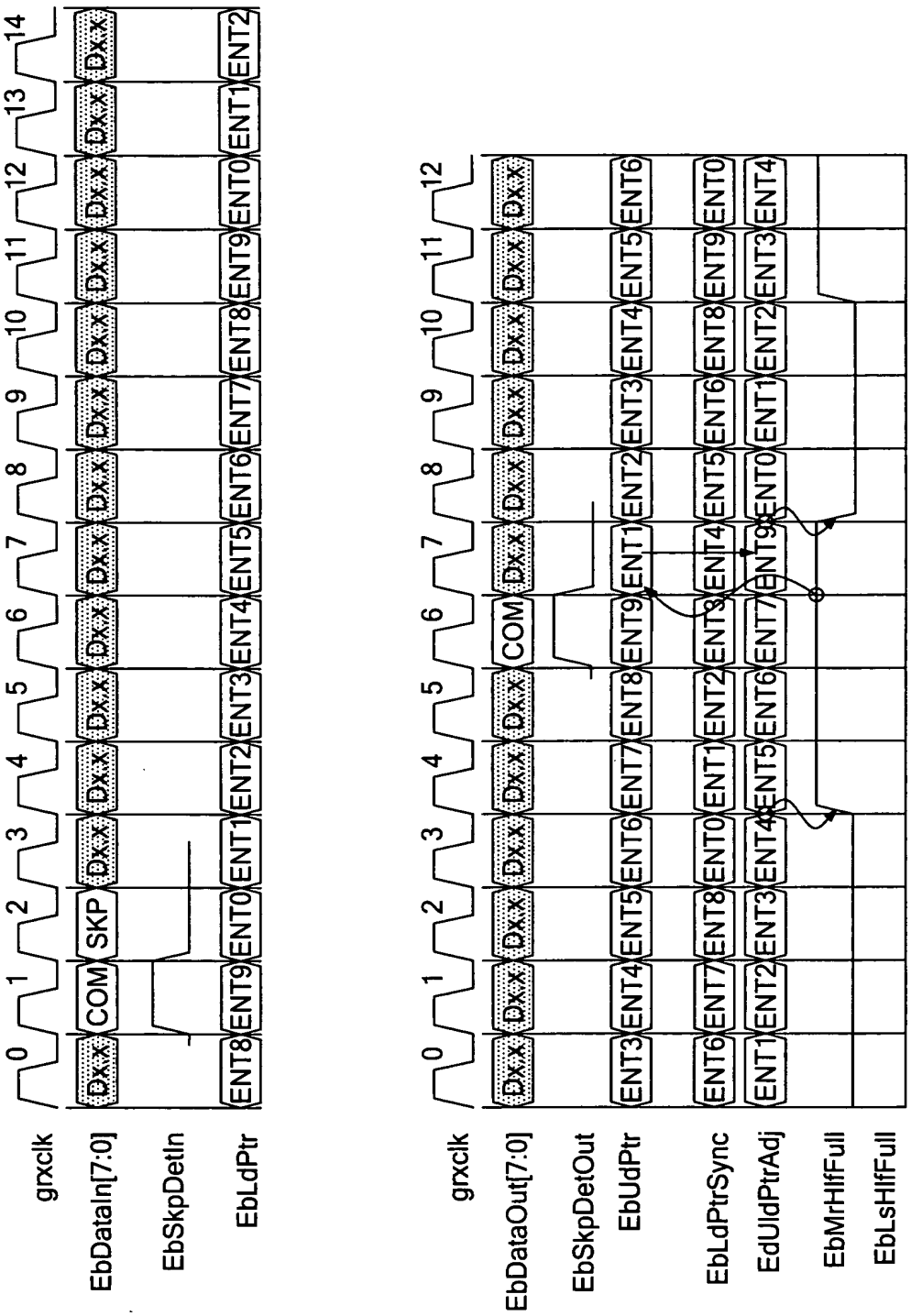
grxclk
EbDataIn[7:0]
EbSkpDetIn
EbLdPtr
EbDataOut[7:0]
EbSkpDetOut
EbUdPtr
EbLdPtrSync
EdUldPtrAdj
EbMrHlfFull
EbLsHlfFull
COM
SKP
Dx.x

Fig.6

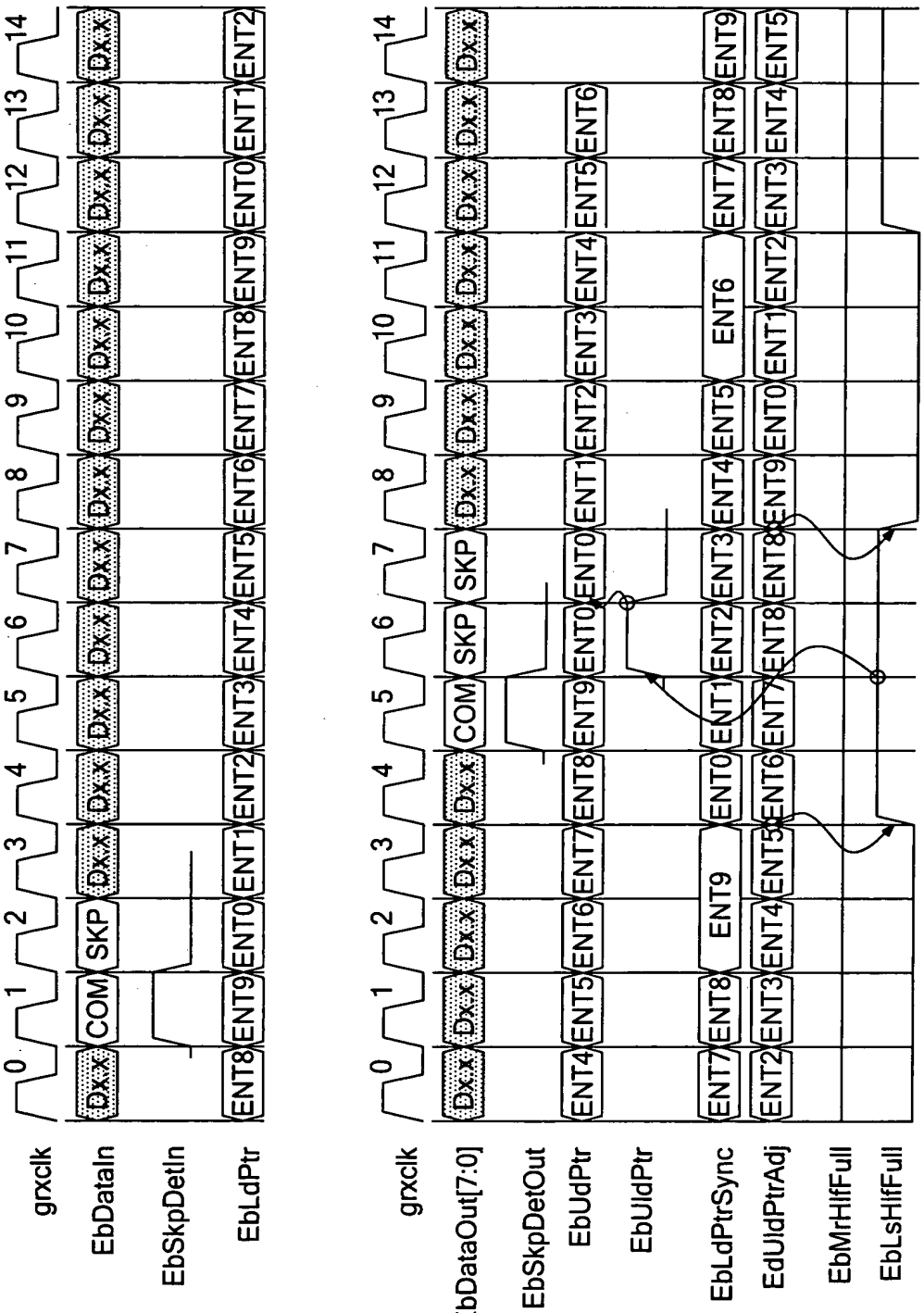
grxclk
EbDataIn
EbSkpDetIn
EbLdPtr
grxclk
EbDataOut[7:0]
EbSkpDetOut
EbUdPtr
EbUldPtr
EbLdPtrSync
EdUldPtrAdj
EbMrHlfFull
EbLsHlfFull

Fig. 7A

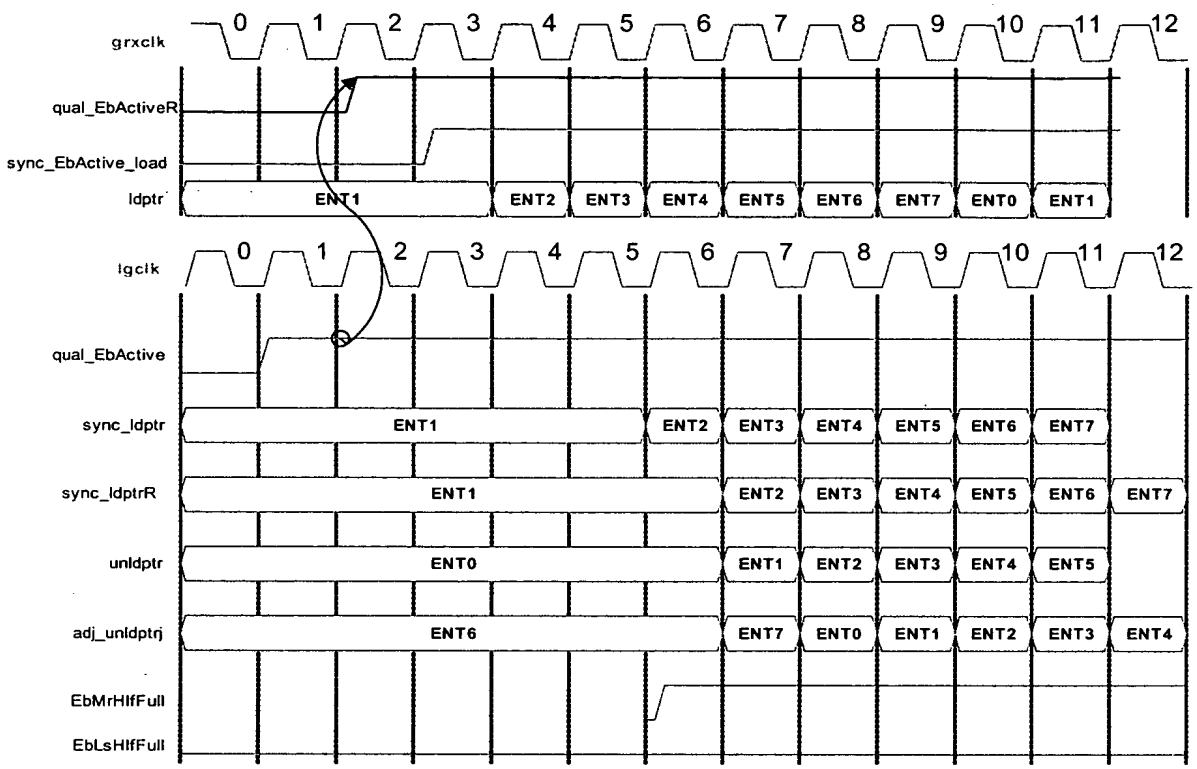
grxclk
qual_EbActiveR
sync_EbActive_load
ldptr
ENT1
ENT2
ENT3
ENT4
ENT5
ENT6
ENT7
ENT0
ENT1
lgclk
qual_EbActive
sync_ldptr
sync_ldptrR
unldptr
adj_unldptrj
EbMrHlfFull
EbLsHlfFull

Fig. 7B

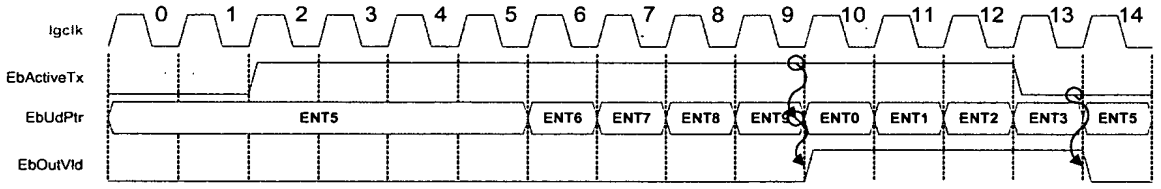
lgclk
EbActiveTx
EbUdPtr
EbOutVld
ENT5
ENT6
ENT7
ENT8
ENT9
ENT0
ENT1
ENT2
ENT3
ENT5

Fig. 7C

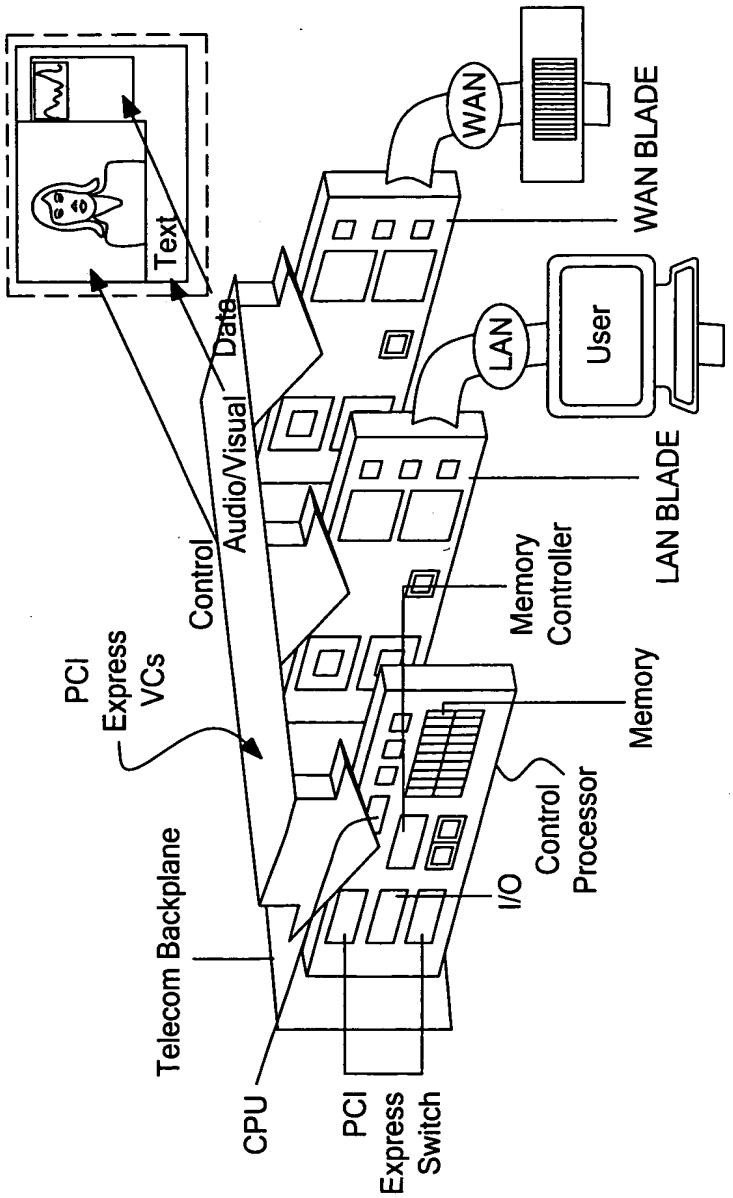
WAN
WAN BLADE
Text
Data
LAN
User
Audio/Visual
Control
LAN BLADE
Memory Controller
PCI Express VCs
Memory
Control Processor
I/O
Telecom Backplane
CPU
PCI Express Switch

Fig.8

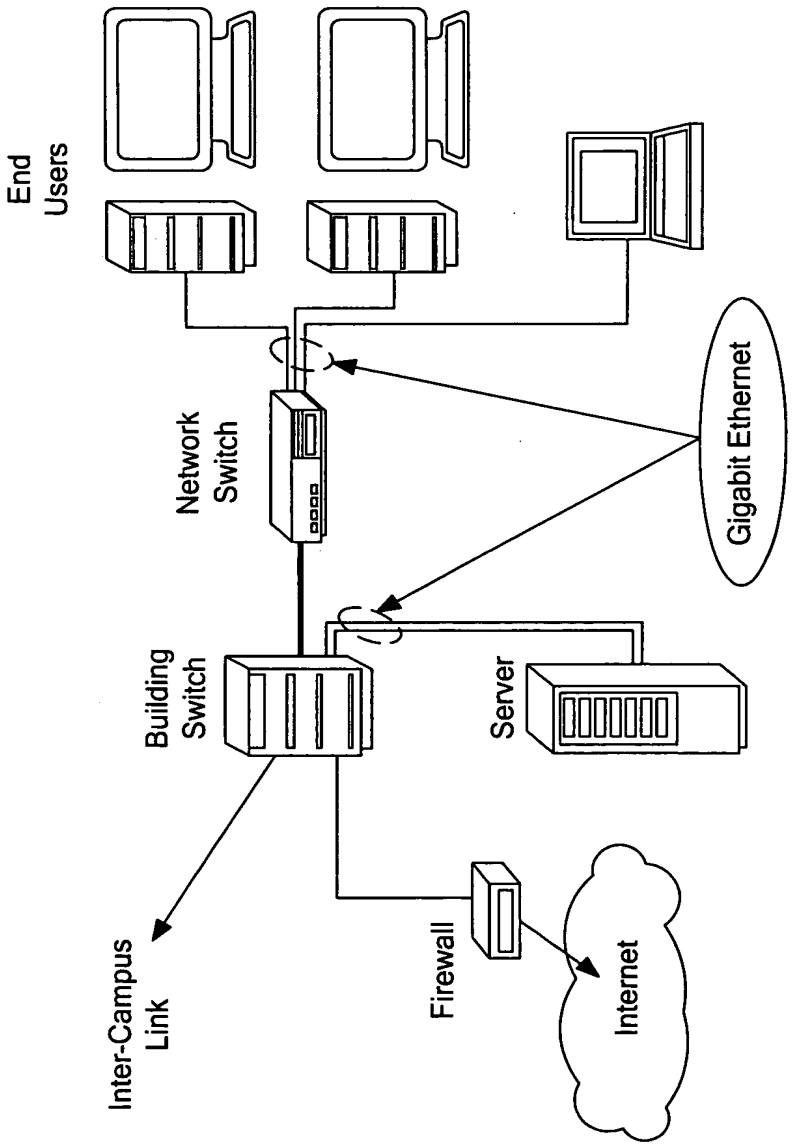
End Users
Network Switch
Gigabit Ethernet
Building Switch
Server
Inter-Campus Link
Firewall
Internet

Fig.9